UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/891,316	06/27/2001	Shotaro Uchida	210093US2S	1655

22850 7590 04/07/2004

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/891,316	UCHIDA, SHOTARO	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2004*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/27/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 21-26 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 21 recites a limitation of " a transistor chip having a first main electrode and a gate electrode for a transistor," implying that a transistor is a (MOS)FET. And Claim 21 further recites a limitation of "one end of the inner lead frame being connected to the main electrode so as to cover at least a part of the Schottky diode." However, with Applicant's remarks filed on January 10, 2004, indicating that 9_2 in Figure 7B is a diode, Figure 7B does not show the one end of the inner lead frame (assuming 29) is connected to the main electrode (15_1) of the transistor (9_1) covers the diode (9_2).

Claim 24 recites a limitation of "the main electrode on at least a part of the diode region." As stated above, Figure 7B dose not shows the one end of the lead frame is connected to the first main electrode (15_1) of the transistor (9_1).

Claims 22 and 25, none of the Figures in the instant invention shows that the first end of the inner lead frame covers the diode entirely. Rather, for example in Figures 7A and 7B show that the inner lead frame (15_1, 15_2) partially covers the device (9_1, 9_2).

Claims 23 and 26 are dependent on the rejected base claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. (US 6144093), hereafter Davis, in view of Watanabe(US 5925926).

Regarding claim 21, Figure 3 of Davis shows a MOSFET 30 having a first source electrode 38 and a gate electrode 36 on an upper surface of the transistor chip, and a Schottky diode 32 formed between the source electrode and the drain electrode as shown in the circuit diagram Figure 6, the bottom surface of the Schottky diode and the drain of MOSFET are electrically connected to a pad 22 (col.3, lines 26-29) and an inner lead frame 28, a first end of the inner lead frame being connected to the main electrode on a part of the diode region, a second end of the inner lead frame being connected to package lead.

In detail, Fig. 3 of Davis shows one end of inner lead portion is connected to the source electrode by a wire bond 42, also connecting the anode of the Schottky diode. Therefore, the wire bond from the end of the inner lead covers a portion of the Schottky diode region.

Also, note that Application simply recites a Schottky diode is connected parallel for a rectifier application. In addition, Fig. 4 of Davis shows the Schottky diode connected parallel to the MOSFET.

Davis shows a structure of the device substantially identical to the claimed invention except an inner lead frame made of a sheet metal. Watanabe discloses a semiconductor packaging device wherein the inner leads are made of sheet metal (col. 3, lines 1-2). It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the teaching of Watanabe for the device of Davis to have inner leads made of sheet metal since using sheet metal for the inner leads improves the mechanical strength for supporting a semiconductor chip.

Regarding claim 24, Figure 3 of Davis shows a MOSFET 30 having a first source electrode 38 and a gate electrode 36 on an upper surface of the transistor chip, and a Schottky diode 32 formed between the source electrode and the drain electrode as shown in the circuit diagram Figure 6, the bottom surface of the Schottky diode and the drain of MOSFET are electrically connected to a pad 22 (col.3, lines 26-29), being electrically coupled to the main electrodes of the transistor and the diode, and an inner lead frame 28, a first end of the inner lead frame being connected to the main electrode on a part of the diode region, a second end of the inner lead frame being connected to package lead.

In detail, Fig. 3 of Davis shows one end of inner lead portion is connected to the source electrode by a wire bond 42, also connecting the anode of the Schottky diode. Therefore, the wire bond from the end of the inner lead covers a portion of the Schottky diode region.

Also, note that Application simply recites a Schottky diode is connected parallel for a rectifier application. In addition, Fig. 4 of Davis shows the Schottky diode connected parallel to the MOSFET.

Davis shows a structure of the device substantially identical to the claimed invention except an inner lead frame made of a sheet metal. Watanabe discloses a semiconductor packaging device wherein the inner leads are made of sheet metal (col. 3, lines 1-2). It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the teaching of Watanabe for the device of Davis to have inner leads made of sheet metal since using sheet metal for the inner leads improves the mechanical strength for supporting a semiconductor chip.

Regarding claims 22 and 25, insofar as understood, Figure 8 of Davis shows that the electrodes (34, 38) cover substantially the entire surface of the devices.

Regarding claims 23 and 26, Figure 8 of Davis shows an N-MOSFET. Alternatively it is obvious to use an NMOS in a semiconductor packaging device since an NMOS is one of the most commonly used semiconductor chip for an IC circuit.

Response to Arguments

Applicant's arguments filed January 9, 2004 have been fully considered but they are not persuasive. New rejections are made modified only to accommodate the amendments/arguments.

In addition, Examiner presents the remarks below in response to Applicant's arguments.

The Applicant states main contention starting on page 8, line 4 " From the above teachings it is clear that the specification ... SBD is covered by an inner lead frame 15_2.

First, the remark of "the semiconductor chips 9_1 and 9_2 are Q2 and Q1 in Figure 8" renders confusing. Since 9_1(or 9_2) in Figure 7A(7B) is one device (a MOSFET or a diode), 9_1 can not be corresponding to a chip Q1(or Q2) with two devices (a MOSFET and a diode). However, Examiner assumes this statement implying that Figures 7A(7B) can be used with a circuit configuration of Q1 or Q2 shown in Figure 8. Therefore, 9_1 (or 9_2) can be a MOSFET or a diode.

Second, with the statement of "SBD is covered by an inner lead frame 15_2," Examiner assumes that a device on the left side (9_2) in Figure 7B is a diode. Then, as pointed out in the Office Action above, Figure 7B does not show one end of the inner lead frame is connected to the main electrode (15_1) of a transistor (9_1; a MOSFET) while the other end connected to a package lead (a portion with 33).

Finally, Applicant asserted that an electrode for example 15_2 is also an inner lead frame. Then, Examiner would like point out that an electrode (an inner lead frame) has to cover a device at least partially.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi

P... ...er
Steven Loke